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Attorney's Docket No. 67,200-506 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Yu
Serial No.: 09/ 920,911
Filed: August 2, 2001
For: Thermal Compensation Method for Forming Semiconductor ... Fabrication

Group Art Unit: 2812
Examiner: Richard A. Booth

Commissioner for Patents
Alexandria, VA 22313

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal Filed on Nov. 3, 2003.

NOTE: "The Appellant shall, within 2 months from the date of the notice of appeal under §1.191(a) or within the time allowed for response to the action appealed from, if such time is later, file a brief in "triplicate", 37 C.F.R. 1.192(a) [emphasis added].

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:

___	small entity	$165.00
X	other than a small entity	$330.00

Appeal Brief fee due: $ 330.00

Certificate of Mailing/Transmission (37 CFR 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 275 480 575 US in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313

Kathy Dixon

Dated: 1/5/04

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of ☐1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) ☐ Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
☐	one month	$ 110.00	$ 55.00
☐	two months	$ 420.00	$210.00
☐	three months	$ 950.00	$475.00
☐	four months	$1,480.00	$740.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) ☐ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief Fee: $ 330.00
Extension fee (if any) $_____

TOTAL FEE DUE: $ 330.00

6. FEE PAYMENT

X Attached is a Credit Card Payment Form for the sum of $ 330.00
X Credit Card Payment Form in the sum of $ 330.00 .
A duplicate copy of this transmittal is attached.

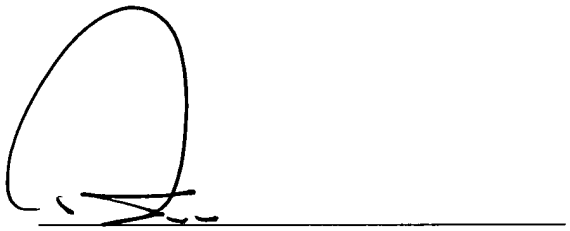
7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

_X_ If any additional extension and/or fee is required, this is a request therefor to charge Deposit Account No. 50-0484

And/Or

_X_ If any additional fee for claims is required, please charge Deposit Account No. 50-0484



Signature of Attorney

Registration No. 31,311

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FROM: Tung & Associates
838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302

DATE: 3 November 2003

REF:

Appellant	:	Yu	Filing Date	:	2 August 2001
Serial No.	:	09/920,911	Att'y No.	:	67,200-506; TSMC 00-804
Art Unit	:	2812	Examiner	:	Richard A. Booth
Title	:	Thermal Compensation Method for Forming Semiconductor Integrated Circuit Microelectronic Fabrication			

EXPRESS MAIL CERTIFICATE

Express Mail label Number EV 275 480 575 US
Date of Deposit Jan. 5/04

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $330.00 (required filing fee) are being deposited with the United States Postal Service via Express Mail on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313

Kathy Dixon

APPEAL BRIEF

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 4 August 2003 and made FINAL, appellant filed a notice of appeal on 3 November 2003. In accord with appellant's notice of appeal, please accept this appeal brief. No oral argument is requested.

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Co., Ltd.
121 Park Avenue, No. 3
Science Based Industrial Park
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 1-19 are pending in this application. No claims have been canceled, allowed, objected to or subject to restriction. Claim 13 is finally rejected under 35 U.S.C. § 112, first paragraph. Claims 1-2, 7-8, 12, 14 and 19 are finally rejected under 35 U.S.C. § 102(b). Claims 3-6, 9-11, 13 and 15-18 are finally rejected under 35 U.S.C. § 103(a).

4. Status of the Amendments

A reply, filed 26 September 2003, was submitted in response to the office action made FINAL, in order to overcome the Examiner's rejections of the claims pending within this application. In an advisory action mailed on 27 October 2003, the Examiner indicated that appellant's response was considered but did not place appellant's application in condition for allowance, for reasons related to those of record.

5. Summary of the Invention

The invention provides a method for forming within a semiconductor integrated circuit microelectronic fabrication a plurality of semiconductor devices having a corresponding plurality of gate dielectric layers having a corresponding plurality of gate dielectric layer

thicknesses, wherein the semiconductor integrated circuit microelectronic fabrication is formed with enhanced manufacturability. (paragraph 0018)

The present invention realizes the foregoing object by first defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps. Similarly, the present invention then provides for sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers, but having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps. Finally, the present invention provides for supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps. Within the present invention, the supplemental thermal annealing provides the semiconductor substrate with a uniform aggregate thermal exposure such that, for example and without limitation, device performance within the semiconductor substrate may be uniformly effected and modeled independently of a number of thermal oxidation process steps to which the semiconductor substrate is exposed. (paragraph 0020)

The invention is claimed in three levels of scope including: (1) a general thermal annealing compensation method in accord with claims 1-7 not otherwise teaching a specific number of gate oxide layers; (2) a more specific thermal annealing compensation method in accord with claims 8-12 teaching a total of three gate oxide layers; and (3) a more specific thermal annealing compensation method in accord with claims 12-19 teaching that appellant's supplemental thermal annealing compensation method provides no additional gate oxide layer.

Independent claim 1 is read on the specification and drawings as follows:

1. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers 14a/18a/22 having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps 16/20/24; (Figs. 1-5 and paragraphs 0030-0049 counted by hand)

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers 34a/34b/42 having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps 36/44; (Figs. 6-9 and paragraphs 0052-0062 counted by hand) and

supplementally thermally annealing 40 the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers 34a/34b/42 having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps 36/44. (Fig. 7 and paragraphs 0054-0056)

6. Issues

I. Whether claim 13 may properly be rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

II. Whether claims 1-2, 7-8, 12, 14 and 19 may properly be rejected under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art.

III. Whether claims 3-6, 9-11, 13 and 15-18 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over appellant's admitted prior art.

7. Grouping of Claims

Claims 1-7 (group I) are directed towards a first claimed embodiment of the invention.

Claims 8-12 (group II) are directed towards a second claimed embodiment of the invention.

Claims 13-19 (group III) are directed towards a third claimed embodiment of the invention.

The claims stand or fall together within their respective groups.

8. Argument

I. Claim 13 may not properly be rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

a. The Examiner's Assertions

At page 2, last paragraph of the office action made FINAL, the Examiner asserts that "[t]he specification, as originally filed, fails to provide support for the limitation of 'supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer' since the supplemental thermal anneal will inherently produce another gate dielectric since it is equivalent to the twice thermally oxidized substrate of the prior art."

At page 4, first paragraph of the office action made FINAL, the Examiner further asserts that appellant's citation of paragraph 0056 as teaching the above supplemental thermal annealing does not overcome the Examiner's rejections since the same does not "compensate for forming thereupon the gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses" as required in appellant's claim 13.

b. Appellant's Response

In response in a first instance, appellant respectfully disagrees with the Examiner's assertion that appellant's specification as originally filed fails to provide support for the limitation "supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer."

Rather, appellant believes that appellant's paragraph 0056 (counted by hand and reproduced below for reference) provides support for appellant's limitation of "supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer."

> "The compensating thermal annealing environment 40 may comprise purely a thermal annealing environment (i.e., an unreactive environment) or in an alternative (and preferably) may comprise an oxidizing thermal annealing environment in accord with the second thermal oxidizing environment 20 as illustrated within the schematic cross-sectional diagram of Fig. 3. Within the preferred embodiment of the present invention, the compensating thermal annealing environment 40 is intended to provide a compensating thermal exposure to the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 7 without forming any independent gate oxide layers therein." (emphasis added)

In accord with the foregoing disclosure, and in particular insofar as appellant's supplemental thermal annealing environment "may comprise purely a thermally annealing environment (i.e., an unreactive environment)" appellant asserts that it is very clearly described in appellant's specification that appellant's supplemental annealing thermal annealing of appellant's semiconductor substrate may be effected "without forming any independent gate oxide layer therein."

In a second instance, and in response to the Examiner's assertion that appellant's citation of paragraph 0056 does not overcome the Examiner's rejections since the same does not "compensate for forming thereupon the gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses" as required in appellant's claim 13, appellant further cites paragraph 0065 (counted by hand and provided below for reference).

> "Upon forming the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrate in Fig. 10, there is provided by the present invention a semiconductor integrated circuit microelectronic fabrication in accord with the preferred embodiment of the present invention. The semiconductor integrated circuit microelectronic fabrication has formed therein devices with gate oxide layers of differing thicknesses of less than a maximum number of differing thicknesses, and with predictable and uniform properties. The foregoing result is realized by providing a compensating thermal annealing treatment to the semiconductor integrated circuit microelectronic fabrication incident to its fabrication. While the compensating thermal treatment is illustrated interposed between forming various gate oxide layers, it may also be provided prior to forming the various gate oxide layers or after forming the various gate oxide layers." (emphasis added)

Paragraph 0065 clearly provides that appellant's supplementary thermal annealing is intended to compensate for forming appellant's gate oxide layers of less than a maximum numbered plurality of differing thicknesses.

In light of the foregoing responses, appellant respectfully submits that appellant's specification clearly supports all aspects of the subject matter claimed within appellant's claim 13, and thus appellant respectfully requests that the Examiner's rejection of claim 13 under 35 U.S.C. § 112, first paragraph, be reversed.

II. Claims 1-2, 7-8, 12, 14 and 19 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art.

III. Claims 3-6, 9-11, 13 and 15-18 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over appellant's admitted prior art.

a. Appellant's Admitted Prior Art

Appellant assumes that the Examiner intends for appellant's admitted prior art that which appellant initially discloses in paragraph 0029 (counted by hand) and reproduced below for reference.

> "Referring now to Fig. 1 to Fig. 5, there is shown a series of schematic cross-sectional diagrams illustrating the results of progressive stages in forming within a semiconductor integrated microelectronic fabrication, and in accord with a generally conventional method, a series of gate dielectric layers. Within the schematic cross-sectional diagrams of Fig. 1 to Fig. 5, the process flow is generally conventional (in accord with disclosures of the Related Art references which are incorporated herein fully by reference), but the process parameters need not be conventional."

The presumed admitted prior art thus includes appellant's Fig.1 to Fig. 5, as well as appellant's disclosure thereof in appellant's specification at paragraphs 0029 to 0047.

b. The Examiner's Assertions

At page 3, first section of the office action made FINAL and within the paragraph bridging pages 2-3 of the office action mailed 24 September 2002, the Examiner reads appellant's admitted prior art onto appellant's independent claim 1.

In so doing, the Examiner asserts that appellant's admitted prior art provides for "supplementally thermally annealing a semiconductor substrate to compensate for forming thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of thermal oxidation process steps," in accord with appellant's claim 1 (clause 3), claim 8 (clause 3) and claim 13 (clause 3).

At page 3, second section of the office action made FINAL and at page 3 of the office action mailed 24 September 2002, the Examiner predicates unpatentability of other of appellant's claims (with respect to both process ordering limitations and parametric limitations) as being obvious absent a showing of new or unexpected results. In so doing, the Examiner cites *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

c. Appellant's Response

In response, appellant respectfully disagrees within the Examiner's reading of appellant's admitted prior art insofar as the Examiner within the paragraph bridging pages 2-3 of the office action mailed on 24 September 2002 characterizes prior art thermal oxidizing process step 24 in appellant's Fig. 5 as a supplemental thermal annealing process step in accord with appellant's claim 1 (clause 3), claim 8 (clause 3) and claim 13 (clause 3).

Rather, prior art thermal oxidizing process step 24 in appellant's Fig. 5 is employed for forming prior art third gate oxide layer 22 upon prior art active region 11c of prior art three times thermally oxidized semiconductor substrate 10"' (page 19, second full paragraph), and is thus not a supplemental thermal annealing process step (absent forming a gate oxide in particular in accord with appellant's claim 13) but rather a non-supplemental thermal oxidizing process step which is employed for forming a specific gate dielectric layer of a specific thickness upon a specific active region of prior art semiconductor substrate Within appellant's admitted prior art as illustrated in Fig. 1 to Fig. 5 and as cited by the Examiner, prior art thermal oxidizing process steps 16, 20 and 24 are employed for forming prior art corresponding gate dielectric layers 14a, 18a and 22 upon prior art corresponding active regions 11a, 11b and 11c of prior art three times thermally oxidized semiconductor substrate 10"', and thus there is no supplemental thermal annealing process step employed within appellant's admitted prior art.

Thus, since each and every limitation within appellant's invention as disclosed and claimed within claim 1, claim 8 and claim 13 is not taught within appellant's admitted prior art, in particular with respect to a supplemental thermal annealing process step for thermally annealing a semiconductor substrate to compensate for forming thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps (and in particular absent forming a gate oxide thereupon in accord with claim 13), appellant asserts that claim 1, claim 8 and claim 13 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art.

Since the remaining claims within the foregoing rejections are dependent upon claim 1, claim 8 or claim 13 and carry all of the limitations of claim 1, claim 8 or claim 13, appellant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art.

In light of the foregoing response, appellant respectfully requests that: (1) the Examiner's rejections of claims 1-2, 7-8, 12, 14 and 19 under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art; and (2) the Examiner's rejections of appellant's claims 3-6, 9-11, 13 and 15-18 under 35 U.S.C. § 103(a) as being unpatentable over appellant's admitted prior art, be reversed.

9. Summary

Appellant's invention as disclosed and claimed within claim 1 and claim 8 is directed towards a method for fabricating a semiconductor substrate to form thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality

of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps. The method employs a supplemental thermal annealing process step, which is absent from appellant's admitted prior art, to compensate for the less than corresponding maximum numbered plurality of thermal oxidation process steps. In addition, and in accord with claim 13, the supplemental thermal annealing process step does not form a gate dielectric layer upon appellant's semiconductor substrate.

10. Conclusion

Appellant requests that the Board of Patent Appeals and Interferences reverse the Examiner's action in rejecting the claims within this application within the office action made FINAL. Allowance of all claims pending within this application, in accord with the appended copy of the claims, is respectfully requested.

Respectfully submitted,

Randy W. Tung (Reg. No. 31,311)

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838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302
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APPENDIX

COMPLETE COPY OF THE CLAIMS

1. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

2. (original) The method of claim 1 wherein the maximum numbered plurality is at least three.

3. (original) The method of claim 1 wherein the maximum numbered plurality is greater than three.

4. (original) The method of claim 1 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

5. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

6. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

7. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

8. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having three differing thicknesses formed employing three thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the three differing thicknesses formed employing less than the three thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having the less than three differing thicknesses formed employing the less than three thermal oxidation process steps.

9. (original) The method of claim 8 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

10. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

11. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

12. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

13. (previously presented) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer thereupon to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

14. (previously presented) The method of claim 13 wherein the maximum numbered plurality is at least three.

15. (previously presented) The method of claim 13 wherein the maximum numbered plurality is greater than three.

16. (previously presented) The method of claim 13 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

17. (previously presented) The method of claim 13 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

18. (previously presented) The method of claim 13 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

19. (previously presented) The method of claim 13 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPEAL BRIEF

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

FROM: Tung & Associates
838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302

DATE: 3 November 2003

REF:

Appellant	:	Yu	Filing Date	:	2 August 2001
Serial No.	:	09/920,911	Att'y No.	:	67,200-506; TSMC 00-804
Art Unit	:	2812	Examiner	:	Richard A. Booth
Title	:	Thermal Compensation Method for Forming Semiconductor Integrated Circuit Microelectronic Fabrication			

EXPRESS MAIL CERTIFICATE

Express Mail label Number EV 275 480 575 US
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I hereby certify that this paper in triplicate and a credit card payment form in the amount of $330.00 (required filing fee) are being deposited with the United States Postal Service via Express Mail on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313

Kathy Dixon

APPEAL BRIEF

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 4 August 2003 and made FINAL, appellant filed a notice of appeal on 3 November 2003. In accord with appellant's notice of appeal, please accept this appeal brief. No oral argument is requested.

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Co., Ltd.
121 Park Avenue, No. 3
Science Based Industrial Park
Hsin-Chu, Taiwan, Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interferences

There are no related appeals or interferences for this United States Patent application.

3. Status of the Claims

Claims 1-19 are pending in this application. No claims have been canceled, allowed, objected to or subject to restriction. Claim 13 is finally rejected under 35 U.S.C. § 112, first paragraph. Claims 1-2, 7-8, 12, 14 and 19 are finally rejected under 35 U.S.C. § 102(b). Claims 3-6, 9-11, 13 and 15-18 are finally rejected under 35 U.S.C. § 103(a).

4. Status of the Amendments

A reply, filed 26 September 2003, was submitted in response to the office action made FINAL, in order to overcome the Examiner's rejections of the claims pending within this application. In an advisory action mailed on 27 October 2003, the Examiner indicated that appellant's response was considered but did not place appellant's application in condition for allowance, for reasons related to those of record.

5. Summary of the Invention

The invention provides a method for forming within a semiconductor integrated circuit microelectronic fabrication a plurality of semiconductor devices having a corresponding plurality of gate dielectric layers having a corresponding plurality of gate dielectric layer

thicknesses, wherein the semiconductor integrated circuit microelectronic fabrication is formed with enhanced manufacturability. (paragraph 0018)

The present invention realizes the foregoing object by first defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps. Similarly, the present invention then provides for sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers, but having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps. Finally, the present invention provides for supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps. Within the present invention, the supplemental thermal annealing provides the semiconductor substrate with a uniform aggregate thermal exposure such that, for example and without limitation, device performance within the semiconductor substrate may be uniformly effected and modeled independently of a number of thermal oxidation process steps to which the semiconductor substrate is exposed. (paragraph 0020)

The invention is claimed in three levels of scope including: (1) a general thermal annealing compensation method in accord with claims 1-7 not otherwise teaching a specific number of gate oxide layers; (2) a more specific thermal annealing compensation method in accord with claims 8-12 teaching a total of three gate oxide layers; and (3) a more specific thermal annealing compensation method in accord with claims 12-19 teaching that appellant's supplemental thermal annealing compensation method provides no additional gate oxide layer.

Independent claim 1 is read on the specification and drawings as follows:

1. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers 14a/18a/22 having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps 16/20/24; (Figs. 1-5 and paragraphs 0030-0049 counted by hand)

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers 34a/34b/42 having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps 36/44; (Figs. 6-9 and paragraphs 0052-0062 counted by hand) and

supplementally thermally annealing 40 the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers 34a/34b/42 having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps 36/44. (Fig. 7 and paragraphs 0054-0056)

6. Issues

I. Whether claim 13 may properly be rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

II. Whether claims 1-2, 7-8, 12, 14 and 19 may properly be rejected under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art.

III. Whether claims 3-6, 9-11, 13 and 15-18 may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over appellant's admitted prior art.

7. Grouping of Claims

Claims 1-7 (group I) are directed towards a first claimed embodiment of the invention.

Claims 8-12 (group II) are directed towards a second claimed embodiment of the invention.

Claims 13-19 (group III) are directed towards a third claimed embodiment of the invention.

The claims stand or fall together within their respective groups.

8. Argument

I. Claim 13 may not properly be rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

a. The Examiner's Assertions

At page 2, last paragraph of the office action made FINAL, the Examiner asserts that "[t]he specification, as originally filed, fails to provide support for the limitation of 'supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer' since the supplemental thermal anneal will inherently produce another gate dielectric since it is equivalent to the twice thermally oxidized substrate of the prior art."

At page 4, first paragraph of the office action made FINAL, the Examiner further asserts that appellant's citation of paragraph 0056 as teaching the above supplemental thermal annealing does not overcome the Examiner's rejections since the same does not "compensate for forming thereupon the gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses" as required in appellant's claim 13.

b. Appellant's Response

In response in a first instance, appellant respectfully disagrees with the Examiner's assertion that appellant's specification as originally filed fails to provide support for the limitation "supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer."

Rather, appellant believes that appellant's paragraph 0056 (counted by hand and reproduced below for reference) provides support for appellant's limitation of "supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer."

> "The compensating thermal annealing environment 40 may comprise purely a thermal annealing environment (i.e., an unreactive environment) or in an alternative (and preferably) may comprise an oxidizing thermal annealing environment in accord with the second thermal oxidizing environment 20 as illustrated within the schematic cross-sectional diagram of Fig. 3. Within the preferred embodiment of the present invention, the compensating thermal annealing environment 40 is intended to provide a compensating thermal exposure to the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrated in Fig. 7 without forming any independent gate oxide layers therein." (emphasis added)

In accord with the foregoing disclosure, and in particular insofar as appellant's supplemental thermal annealing environment "may comprise purely a thermally annealing environment (i.e., an unreactive environment)" appellant asserts that it is very clearly described in appellant's specification that appellant's supplemental annealing thermal annealing of appellant's semiconductor substrate may be effected "without forming any independent gate oxide layer therein."

In a second instance, and in response to the Examiner's assertion that appellant's citation of paragraph 0056 does not overcome the Examiner's rejections since the same does not "compensate for forming thereupon the gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses" as required in appellant's claim 13, appellant further cites paragraph 0065 (counted by hand and provided below for reference).

> "Upon forming the semiconductor integrated circuit microelectronic fabrication whose schematic cross-sectional diagram is illustrate in Fig. 10, there is provided by the present invention a semiconductor integrated circuit microelectronic fabrication in accord with the preferred embodiment of the present invention. The semiconductor integrated circuit microelectronic fabrication has formed therein devices with gate oxide layers of differing thicknesses of less than a maximum number of differing thicknesses, and with predictable and uniform properties. The foregoing result is realized by providing a compensating thermal annealing treatment to the semiconductor integrated circuit microelectronic fabrication incident to its fabrication. While the compensating thermal treatment is illustrated interposed between forming various gate oxide layers, it may also be provided prior to forming the various gate oxide layers or after forming the various gate oxide layers." (emphasis added)

Paragraph 0065 clearly provides that appellant's supplementary thermal annealing is intended to compensate for forming appellant's gate oxide layers of less than a maximum numbered plurality of differing thicknesses.

In light of the foregoing responses, appellant respectfully submits that appellant's specification clearly supports all aspects of the subject matter claimed within appellant's claim 13, and thus appellant respectfully requests that the Examiner's rejection of claim 13 under 35 U.S.C. § 112, first paragraph, be reversed.

II. Claims 1-2, 7-8, 12, 14 and 19 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art.

III. Claims 3-6, 9-11, 13 and 15-18 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over appellant's admitted prior art.

a. Appellant's Admitted Prior Art

Appellant assumes that the Examiner intends for appellant's admitted prior art that which appellant initially discloses in paragraph 0029 (counted by hand) and reproduced below for reference.

> "Referring now to Fig. 1 to Fig. 5, there is shown a series of schematic cross-sectional diagrams illustrating the results of progressive stages in forming within a semiconductor integrated microelectronic fabrication, and in accord with a generally conventional method, a series of gate dielectric layers. Within the schematic cross-sectional diagrams of Fig. 1 to Fig. 5, the process flow is generally conventional (in accord with disclosures of the Related Art references which are incorporated herein fully by reference), but the process parameters need not be conventional."

The presumed admitted prior art thus includes appellant's Fig.1 to Fig. 5, as well as appellant's disclosure thereof in appellant's specification at paragraphs 0029 to 0047.

b. The Examiner's Assertions

At page 3, first section of the office action made FINAL and within the paragraph bridging pages 2-3 of the office action mailed 24 September 2002, the Examiner reads appellant's admitted prior art onto appellant's independent claim 1.

In so doing, the Examiner asserts that appellant's admitted prior art provides for "supplementally thermally annealing a semiconductor substrate to compensate for forming thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of thermal oxidation process steps," in accord with appellant's claim 1 (clause 3), claim 8 (clause 3) and claim 13 (clause 3).

At page 3, second section of the office action made FINAL and at page 3 of the office action mailed 24 September 2002, the Examiner predicates unpatentability of other of appellant's claims (with respect to both process ordering limitations and parametric limitations) as being obvious absent a showing of new or unexpected results. In so doing, the Examiner cites *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

c. Appellant's Response

In response, appellant respectfully disagrees within the Examiner's reading of appellant's admitted prior art insofar as the Examiner within the paragraph bridging pages 2-3 of the office action mailed on 24 September 2002 characterizes prior art thermal oxidizing process step 24 in appellant's Fig. 5 as a supplemental thermal annealing process step in accord with appellant's claim 1 (clause 3), claim 8 (clause 3) and claim 13 (clause 3).

Rather, prior art thermal oxidizing process step 24 in appellant's Fig. 5 is employed for forming prior art third gate oxide layer 22 upon prior art active region 11c of prior art three times thermally oxidized semiconductor substrate 10"' (page 19, second full paragraph), and is thus not a supplemental thermal annealing process step (absent forming a gate oxide in particular in accord with appellant's claim 13) but rather a non-supplemental thermal oxidizing process step which is employed for forming a specific gate dielectric layer of a specific thickness upon a specific active region of prior art semiconductor substrate Within appellant's admitted prior art as illustrated in Fig. 1 to Fig. 5 and as cited by the Examiner, prior art thermal oxidizing process steps 16, 20 and 24 are employed for forming prior art corresponding gate dielectric layers 14a, 18a and 22 upon prior art corresponding active regions 11a, 11b and 11c of prior art three times thermally oxidized semiconductor substrate 10"', and thus there is no supplemental thermal annealing process step employed within appellant's admitted prior art.

Thus, since each and every limitation within appellant's invention as disclosed and claimed within claim 1, claim 8 and claim 13 is not taught within appellant's admitted prior art, in particular with respect to a supplemental thermal annealing process step for thermally annealing a semiconductor substrate to compensate for forming thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps (and in particular absent forming a gate oxide thereupon in accord with claim 13), appellant asserts that claim 1, claim 8 and claim 13 may not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art.

Since the remaining claims within the foregoing rejections are dependent upon claim 1, claim 8 or claim 13 and carry all of the limitations of claim 1, claim 8 or claim 13, appellant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art.

In light of the foregoing response, appellant respectfully requests that: (1) the Examiner's rejections of claims 1-2, 7-8, 12, 14 and 19 under 35 U.S.C. § 102(b) as being anticipated by appellant's admitted prior art; and (2) the Examiner's rejections of appellant's claims 3-6, 9-11, 13 and 15-18 under 35 U.S.C. § 103(a) as being unpatentable over appellant's admitted prior art, be reversed.

9. Summary

Appellant's invention as disclosed and claimed within claim 1 and claim 8 is directed towards a method for fabricating a semiconductor substrate to form thereupon a plurality of gate dielectric layers having less than a corresponding maximum numbered plurality

of differing thicknesses formed employing less than a corresponding maximum numbered plurality of thermal oxidation process steps. The method employs a supplemental thermal annealing process step, which is absent from appellant's admitted prior art, to compensate for the less than corresponding maximum numbered plurality of thermal oxidation process steps. In addition, and in accord with claim 13, the supplemental thermal annealing process step does not form a gate dielectric layer upon appellant's semiconductor substrate.

10. Conclusion

Appellant requests that the Board of Patent Appeals and Interferences reverse the Examiner's action in rejecting the claims within this application within the office action made FINAL. Allowance of all claims pending within this application, in accord with the appended copy of the claims, is respectfully requested.

Respectfully submitted,

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APPENDIX

COMPLETE COPY OF THE CLAIMS

1. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

2. (original) The method of claim 1 wherein the maximum numbered plurality is at least three.

3. (original) The method of claim 1 wherein the maximum numbered plurality is greater than three.

4. (original) The method of claim 1 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

5. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

6. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

7. (original) The method of claim 1 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

8. (original) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having three differing thicknesses formed employing three thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the three differing thicknesses formed employing less than the three thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate to compensate for forming thereupon the plurality of gate dielectric layers having the less than three differing thicknesses formed employing the less than three thermal oxidation process steps.

9. (original) The method of claim 8 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

10. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

11. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

12. (original) The method of claim 8 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.

13. (previously presented) A method for fabricating a semiconductor substrate comprising:

defining a sequential and repetitive thermal oxidation and partial stripping method for forming upon a semiconductor substrate a plurality of gate dielectric layers having a maximum numbered plurality of differing thicknesses formed employing a corresponding maximum numbered plurality of thermal oxidation process steps;

sequentially and repetitively thermally oxidizing and partially stripping the semiconductor substrate to form thereupon the plurality of gate dielectric layers having less than the maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps; and

supplementally thermally annealing the semiconductor substrate without forming a gate dielectric layer thereupon to compensate for forming thereupon the plurality of gate dielectric layers having less than the corresponding maximum numbered plurality of differing thicknesses formed employing less than the corresponding maximum numbered plurality of thermal oxidation process steps.

14. (previously presented) The method of claim 13 wherein the maximum numbered plurality is at least three.

15. (previously presented) The method of claim 13 wherein the maximum numbered plurality is greater than three.

16. (previously presented) The method of claim 13 wherein the plurality of differing thicknesses encompass a range including a low thickness of from about 10 to about 40 angstroms and a high thickness of from about 50 to about 200 angstroms.

17. (previously presented) The method of claim 13 wherein the supplemental thermal annealing is undertaken prior to forming the plurality of gate dielectric layers upon the semiconductor substrate.

18. (previously presented) The method of claim 13 wherein the supplemental thermal annealing is undertaken interposed between forming the plurality of gate dielectric layers upon the semiconductor substrate.

19. (previously presented) The method of claim 13 wherein the supplemental thermal annealing is undertaken subsequent to forming the plurality of gate dielectric layers upon the semiconductor substrate.